

1                    **Circuit and Method For Trimming Locking of Integrated Circuits**

2                    The present application claims the benefit of U.S. Provisional Application Serial  
3                    No. 60/471,205, filed May 16, 2003.

4                    **1. Field of the Invention**

5                    The present invention relates to integrated circuits using after-assembly trimming  
6                    procedure, and more particularly, to power management integrated controllers using  
7                    after-assembly trimming procedure.

8                    **2. Background of the Invention**

9                    Conventional post-assembly IC trimming procedures generally end with a locking  
10                  step, designed to disconnect the trimming block from the package pins, making these pins  
11                  available for other functions, and disable permanently the trimming block, while  
12                  preserving the trimmed parameter values status. The post-assembly trimming procedure  
13                  results in an IC with stable parameters, which cannot be further modified through  
14                  accidentally trimming. Conventional IC trimming circuitry is described in Figure 1 and  
15                  Figure 2. Figure 1 shows an IC with a single voltage supply PIN A (VCC) 5, while  
16                  Figure 2 shows an IC with two voltage supplies, PIN A (VCC) 5, AND PIN B (LVCC) 6.  
17                  The energy necessary to change the fuse status is supplied by VCC\_Trimming node 8,  
18                  which is connected either to PIN A 5 or PIN B 6. The programmable fuse (or Zener  
19                  diodes) array 2 is addressed by the input trimming data 9. This input data includes  
20                  conventional data to address programmable fuses (or Zener diodes). The output of each  
21                  individual fuse can be obtained from the fuse status outputs 10 of the programmable fuse  
22                  array block 2. Each fuse cell 4 typically includes a fuse (or Zener diode), a means to

1 change the fuse status (typically a switch controlled by the input trimming data 9), and a  
2 sensing block (not shown) that provides the fuse status output 10.

3 Conventional techniques for trimming locking is provided in, for example, U.S.  
4 Pat. No. 5,079,516 Russell, et al., U.S. Pat. No. 6,472,897 Shyr, et al., U.S. Pat. No.  
5 6,338,032 Chen, and/or France Pat.No. 9908240 Laville et al. As a general matter, these  
6 patents operate by inhibiting the input trimming data transmission from the package pins  
7 to the programmable fuse array block 2.

8 The switch in the fuse cell 4 can include a generic a MOS transistor or a SCR  
9 device. Once the fuse is set (blown), the switch cannot be turned on by means of the  
10 control terminal; therefore the fuse status cannot be changed once set. The major  
11 drawback of this approach is that the fuse (or Zener diode) and the controllable switch in  
12 fuse cell 4 remain connected to the package pins after the trimming procedure is  
13 completed. A subsequent abnormal voltage (over voltage, high dv/dt voltage spike,  
14 electro-static discharge (ESD) spike) on pin A 5 or on pin B 6 may parasitically turn on  
15 the switch in fuse cell 4 (for example, by a break-over, snap-back, and/or drain-gate  
16 capacitance effect), and accidentally blow out the corresponding fuse (or short-circuit the  
17 Zener diode), changing the original trimming procedure results. This means that the  
18 above locking methods are not entirely secure against possible environmental voltage  
19 conditions.

20 In another trimming locking approach, described in U.S. Pat. No. 5,079,516  
21 Russell, et al., two fuses have to be blown out, for each trimmed bit. Two SCR devices  
22 are also needed for locking each trimmed bit. Thus, this method tends to be complicated  
23 and larger chip area is consumed. Moreover, this type of locking procedure based on

1 blown out fuses tends to be only applicable for cavity containing packages, i.e., plastic  
2 packages typically cannot use this locking approach.

3 **Summary of the Invention**

4 The goal of the present invention is to provide the integrated circuits in either  
5 plastic or cavity containing package, and using a post-assembly trimming procedure a  
6 trimming locking circuit and method that secures the trimming status against subsequent  
7 electrical events. The circuit and method of the present invention may be adapted to  
8 change the physical path for delivering the energy to the programmable fuses. Therefore,  
9 neither the normal trimming procedure, nor any electrical event that may exceed the  
10 normal operating conditions (ESD, EOS) will modify the fuse, thereby locking the  
11 trimming status. The present invention may also be used in integrated circuits  
12 encapsulated in plastic or cavity containing package. The present invention may also use  
13 the post assembly trimming pins, and therefore implementation of the present invention  
14 can be accomplished without requiring supplementary pins. The present invention may  
15 be implemented with a low component count. For example, in exemplary embodiments  
16 described herein the present invention can be implemented using three or four  
17 supplementary integrated elements only: a metal fuse, one or two diodes, and one  
18 resistor. The present invention can also be adapted to be used in conjunction with an  
19 after-assembly trimming procedure that implements poly-silicon fuses or Zener diodes to  
20 encode the trimming data.

21 In one exemplary embodiment, a trimming blocking circuit is provided adapted  
22 for use with a single power supply. In this embodiment, a trimming locking circuit is  
23 provided in an integrated circuit with a programmable fuse array that includes a metal

1      fuse and a first blocking diode coupled in series to an input pin; a second blocking diode  
2      and a supply resistor coupled in parallel to a power supply; and wherein said metal fuse,  
3      said supply resistor and said blocking diodes adapted to electrically isolate a load from  
4      over voltage conditions present on said input pin.

5              In another exemplary embodiment, a trimming blocking circuit is provided  
6      adapted for use with a two (or more) power supplies. In this embodiment, a trimming  
7      locking circuit is provided in an integrated circuit with a programmable fuse array that  
8      includes a metal fuse and a supply resistor coupled in parallel, and coupled between a  
9      second power supply and a programmable fuse array supply line; a blocking diode  
10     coupled in reverse bias between said metal fuse and said supply resistor and a first power  
11    supply; and wherein said metal fuse, said supply resistor and said diode adapted to  
12    electrically isolate a load from over voltage conditions present on said second power  
13    supply.

14              It will be appreciated by those skilled in the art that although the following  
15    Detailed Description will proceed with reference being made to preferred embodiments  
16    and methods of use, the present invention is not intended to be limited to these preferred  
17    embodiments and methods of use. Rather, the present invention is of broad scope and is  
18    intended to be limited as only set forth in the accompanying claims.

19              Other features and advantages of the present invention will become apparent as  
20    the following Detailed Description proceeds, and upon reference to the Drawings,  
21    wherein like numerals depict like parts, and wherein:  
22    **Brief Description of the Drawings**

23              Figure 1 is a circuit diagram of a conventional IC trimming circuit;

1       Figure 2 is a circuit diagram of another conventional IC trimming circuit;

2       Figure 3 is a circuit diagram of one exemplary trimming circuit according to the

3    present invention;

4       Figure 4 is a circuit diagram of another exemplary trimming circuit according to

5    the present invention; and

6       Figure 5 is a circuit diagram of an exemplary programmable fuse array according

7    to the present invention.

8    **Detailed Description of Exemplary Embodiments**

9       The object of the present invention is described below, with reference to the

10   Figures 3, 4, and 5, which represent the main blocks of exemplary embodiments of the

11   invention. The trimming locking method and circuit is described for two IC types: one

12   voltage supply ICs (Figures 4, and 5), and two or more voltage supplies ICs (Figures 3,

13   and 5). Broadly stated, the present invention provides a locking trimming circuit that

14   includes inserting a metal fuse across the power path to the programmable fuse array

15   (poly-silicon fuses or Zener diodes). The metal fuse is selected to sustain the current

16   needed to blow out the poly-silicon fuses or Zener diodes. The metal fuse is blown out

17   using a circuit configuration that is also the object of the present invention. Once the

18   metal fuse is blown out, the energy that can flow to the programmable fuse (poly-silicon

19   fuses or Zener diodes as well) array is limited, so the possibility of a parasitic blow out of

20   a fuse is substantially reduced. In other words, no subsequent parasitic voltage can

21   deliver enough energy to the programmable fuse array, therefore the trimming results are

22   safely preserved. The present invention is intended for any integrated circuit that uses a

1 trim process to set the value of one or more voltage/current signals associated with the  
2 IC.

3 Figure 4 depicts an exemplary trimming circuit 100 that uses one metal fuse 33,  
4 two diodes DLOCK1 32, and DLOCK2 31, and one supply resistor 34. The trimming  
5 circuit 100 of Figure 4 is an example of a trim locking circuit according to the present  
6 invention with a single power supply. This circuit is adapted to lock the trimming  
7 process, regardless of the number of bits (fuse cells 4) that are trimmed. A detailed block  
8 diagram of an exemplary fuse cell 4 is depicted in Figure 5.

9 The supply power for the programmable fuse array 2 is supplied during the  
10 post-assembly trimming process to the local supply line VCC\_Trimming 8 from PIN C  
11 14 (typically an input pin of the IC that is not involved in the trimming procedure),  
12 through the DLOCK2 diode 31 in series with the metal fuse 33. A conventional  
13 trimming process is conducted through the input trimming data signals 9, which are  
14 supplied to the switches 42 (Figure 5) through a very high impedance path (for example,  
15 MOS gates 46). The programmable fuse array outputs signals 10, through very high  
16 impedance path (e.g., MOS gates). PIN A (VCC) 5 provides the normal IC power  
17 supply, and can be tied together with PIN C (Input) 14 during the trimming process.

18 Once the trimming process is complete, PIN A (VCC) 5 is connected to the  
19 ground GND 7, and the PIN C 14 voltage is raised a sufficient amount so the current  
20 necessary to blow out the metal fuse 33 can flow from PIN C 14 through DLOCK2 31,  
21 Metal fuse 33, and DLOCK1 32 to PIN A (VCC) 5. After the metal fuse 33 is blown, the  
22 local VCC-Trimming line 8 is supplied from PIN A (VCC) 5, through the supply resistor  
23 34. The supply current for the programmable fuse array 2 is only necessary to detect the

1 trimmed fuses status, and therefore the supply resistor 34 can be set to a large value,  
2 depending on, for example, the current requirements of the fuse array.

3 Over voltage on nodes PIN C 14, and PIN A 5 is limited during an ESD event by  
4 the regular ESD devices 13, and 12. Finally, after the metal fuse 33 is blown out, the  
5 programmable fuse array 2 remains only coupled to the package pins through the supply  
6 resistor 34. The resistance value of the supply resistor 34 is selected to be large enough  
7 so a parasitic over voltage (limited by the ESD device 12) on PIN A (VCC) 5 cannot  
8 transfer the necessary energy to the local supply line 8 to possibly blow out one or more  
9 trimming fuses in the fuse cell 4. This provides the after-assembly trimming locking  
10 against possible subsequent over-voltage events. The input on PIN C 14 is electrically  
11 isolated from the programmable fuse array 2 when the metal fuse 33 is blown (described  
12 above). Also, PIN C is isolated due to the blocking effect of diode DLOCK2 31. PIN C  
13 14 can be used for the second function it was intended for (Input). After the metal fuse  
14 33 is blown, only a limited energy can be supplied to the programmable fuse array 2,  
15 either through the supply resistor (high resistance) or through the residual resistance of  
16 the blown metal fuse (high resistance, even for plastic package).

17 The concept is therefore applicable to the plastic packaged ICs as well. Even if  
18 the metal fuse 33 is not blown completely, its remaining resistance will typically be large  
19 enough, and therefore energy transferred through this path during an over voltage event  
20 typically cannot affect the programmable fuses in the fuse cells 4.

21 Referring now to Figure 3, another exemplary trimming circuit 200 that uses one  
22 metal fuse 21, one diode DLOCK 22, and one supply resistor 23 is depicted. The  
23 trimming circuit 200 of Figure 3 is an example of a trim locking circuit according to the

1 present invention with two power supplies. This circuit is adapted to lock the trimming  
2 process, regardless of the number of bits (fuse cells 4) that are trimmed. A detailed block  
3 diagram of an exemplary fuse cell 4 is depicted in Figure 5.

4 The supply power for the programmable fuse array 2 during the post-assembly  
5 trimming process is supplied to the local supply line VCC\_Trimming 8 from PIN B  
6 (LVCC) 6 (typically an secondary constant voltage, lower than VCC) through the metal  
7 fuse 21. The trimming process using conventional techniques (described above) supplies  
8 the Input Trimming Data signals 9 to the switches 42 in Figure 5 through a very high  
9 impedance path (MOS gates 46). Once the trimming process is complete, PIN A (VCC)  
10 5 is connected to the ground GND 7, and the PIN B 6 voltage is increased, so the current  
11 necessary to blow out the metal fuse 21 can flow through the metal fuse 21, and DLOCK  
12 diode 22 to PIN A (VCC) 5 pin.

13 After the metal fuse 33 is blown, the local VCC-Trimming line 8 is supplied from  
14 PIN B (LVCC) 6, through the supply resistor 23. The supply current for the  
15 programmable fuse array is only necessary to detect the trimmed fuse status, and  
16 accordingly, the supply resistor can be selected to an appropriate large value, depending  
17 on, for example, the current requirements of the fuse array.

18 Finally, after the metal fuse 23 is blown, the programmable fuse array 2 remains  
19 only coupled to the package pins through the supply resistor 23, which is selected large  
20 enough so that a parasitic over voltage (limited by the ESD device 11) on PIN B (LVCC)  
21 6 will have no effect upon the fuses in the programmable fuse array 2.

22 Therefore, accidental energy transfer to the local supply line 8 (which can  
23 possibly blow out one or more trimming fuses in the fuse cell 4) is likewise prevented.

1 PIN B 6 can be used afterwards for the main function for which it was intended ( in this  
2 example PIN B is used as constant voltage supply pin). The concept is equally applicable  
3 to the plastic packaged ICs . Even if the metal fuse 21 is not completely blown open, its  
4 remaining resistance is larger than the resistance of the supply resistor 23, and the  
5 supplied energy transferred through this path during an over voltage event will not affect  
6 the programmable fuses in the fuse cells 4.

7 Those skilled in the art will recognize numerous modifications which may be  
8 made to the present invention. For example, the present invention describes a trimming  
9 locking circuit that is used in conjunction with a programmable fuse array 2. However,  
10 the present invention can be applied to any load, and thus, the programmable fuse array  
11 may be generalized herein as a load. Additionally, a description of a single and dual  
12 power supply topologies is provided herein, but the present invention is equally  
13 extendable to any number of power supplies.

14 Also, supply resistor described above with reference to Figures 3 and 4 is stated  
15 as having a relatively large resistance value, based on for example, the current  
16 requirements of the programmable fuse array 2. The exact resistance value of the supply  
17 resistor 34 or 23 will vary based on the operating environment, the selected application,  
18 and the desired component tolerance. Therefore, the term “large” or “relatively large” in  
19 reference to the resistance value of the supply resistor should be construed broadly to  
20 mean any selected value that will lock the programmable fuse array in accordance with  
21 the principles set forth herein. All such modifications are deemed within the spirit and  
22 scope of the present invention, only as limited by the claims.